SAE International

SURFACE VEHICLE RECOMMENDED PRACTICE

SAE J2628 JUL2013

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Superseding J2628 JUL2007

(R) Characterization, Conducted Immunity

RATIONALE

This revision includes corrections, clarifications and simplifications from July 2007 version, deletion of some tests (transient B1, B2) and addition of transient A2-a and reference to new version of SAE J1211.

FOREWORD

This document establishes methods for characterizing the robustness of vehicle electronic modules to certain electrical and temperature environmental stresses using methods designed to address the deficiencies inherent in other commonly used validation methods. It is an extension of the philosophy detailed in a new SAE document J1211 (see ref 2.2.1) which was developed by the SAE International Automotive Electronic Systems Reliability Standards Committee and ZVEI (German Electrical and Electronic Manufacturers` Association). It can be summarized from this quote from the handbook.

"Robustness Validation relies first on knowledge-based modeling simulation and analysis methods to develop a highly capable design prior to building and testing physical parts; and then on test-to-failure (or acceptable degradation) and failure/defect susceptibility testing to confirm or identify Robustness Margins, to enable failure prediction and verify that manufacturing processes produce defect free parts. These techniques represent advancement beyond "test-to-pass" qualification plans which usually provide very little useful engineering information about failure modes, failure mechanisms and failure points".

1. SCOPE

The methods included in this document are:

a. Voltage-Temperature Design Margins.

b. Voltage Interruptions and Transients.

c. Voltage Dropouts and Dips.

d. Current Draw Under a Number of Conditions.

e. Switch Input Noise

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These methods are best applied during the Development stage but can be used at all stages (e.g., Pre-Qualification, Qualification or Conformity).

1.1 Measurement Philosophy

The main issues associated with contemporary mature electronic systems (non mechanical) are:

a. Requirements not properly defined (e.g., functionality, environment).

b. System interfaces.

c. Trouble Not Indicated (TNI).

A typical validation test program may not sufficiently address these issues. Some common deficiencies are:

a. Requirements validation - tested under ideal conditions (e.g., room temp, bench power supply).

b. Environmental (non EMC) testing mainly wear-out oriented.

c. EMC testing not realistic - room temp only, idealized noise signals.

d. System interactions, interfaces and degradation not sufficiently addressed.

This document addresses much of the above using relatively simple and low cost techniques which:

a. Requires minimal lab facilities.

b. Allows maximum flexibility to experiment early in the program.

c. Allows sufficient reaction time to react to potential issues.

d. Stage where failures are good (maximizes information).

One main issue addressed here is Conducted Immunity (CI). That aspect of Electromagnetic Compatibility (EMC) has the highest potential for warranty and customer satisfaction issues. However, traditional validation testing for CI has major limitations. Specifically, CI testing is most often run at room temperature due to the nature of the test equipment and facilities - the response of the product could be different when cold or hot than at room temperature. Another limitation is that very repeatable, accurate and idealized signals are used to represent the “real world”. While this would appear to be desirable, it is not necessarily the case. The “real world” contains randomness and other characteristics (e.g., complex impedances) not replicated by such idealized test signals. Randomness is extremely critical for a microprocessor type DUT since the stress event (e.g., transients) must often line up in time with a certain point(s) in software execution to have an effect.

It is important to note that many of these tests are not the “test for success” type where the results are classified as either pass or fail. Such testing is of limited value since it generates little information. The goal is to generate variable data or anomalies so that the maximum amount of information is obtained and an informed engineering judgement can be made.

2. REFERENCES

2.1 Applicable Document

The following publication forms a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of publications shall apply.

2.1.1 SAE Publication

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1113-1 Electromagnetic Compatibility Measurement Procedures and Limits for Components of Vehicles, Boats (up to 15 m), and Machines (Except Aircraft) (16.6 Hz to 18 GHz)

2.2 Related Publications

The following publications are provided for information purposes only and are not a required part of this SAE Technical Report.

2.2.1 SAE Publication

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1113-11 Immunity to Conducted Transients on Power Leads

SAE J1211 Handbook for Robustness Validation of Automotive Electrical/Electronic Modules

2.2.2 ISO Publication

Available from American National Standards Institute, 25 West 43rd Street, New York, NY 10036-8002, Tel: 212-642-4900, www.ansi.org.

ISO 7637-2 Road vehicles—Electrical disturbances from conduction and coupling—Electrical transient conduction along supply lines only

2.2.3 IEEE Publication

Comparison of ISO 7637 Transient Waveforms to Real World Automotive Transient Phenomena, 2005 IEEE EMC Symposium

2.2.4 Ford Publication

EMC Specification EMC-CS-2009.1 available at www.fordemc.com

3. DEFINITIONS

3.1 LOL, -X (Y), UOL-X (Y) - See Figure 1

Lower and Upper Operating Limit (when DUT ceases to operate or is erratic) for parameter X at specified conditions Y. For example LOL-V (T-hi) = Lower Operating Limit for voltage at T-hi temperature.

3.2 Tx, Ty - See Figure 1

T1, T2 = Lower /Upper temperature for guaranteed operation (minimun function). T3, T4 = Lower and Upper temperature for guaranteed performance (meets all specs).

3.3 Trouble Not Indicated (TNI)

Potentially defective modules (e.g., field return) where the cause of concern cannot be identified with traditional test methods.

3.4 Vx, Vy - See Figure 1

V1, V2 = Lower and Upper voltage for guaranteed performance (meets all spec). V3, V4 = Lower/Upper voltage for guaranteed operation (minimum function).

4. REQUIREMENTS DESCRIPTION

4.1 Voltage-Temperature Design Margins

This method evaluates Design Margins for voltage over temperature. It can be combined with noise immunity (see 4.2). This testing is especially useful for evaluating electronic design changes or degradation by comparing results before and after other stresses (e.g., thermal cycling). By testing beyond spec limits, it can force failures that would only show up over time in the field (e.g., electrolytic capacitor degradation over time). The data can be used to give a graphical representation comparing the DUT specification limits (voltage, temp) with the Design Margin envelope (figure 1).

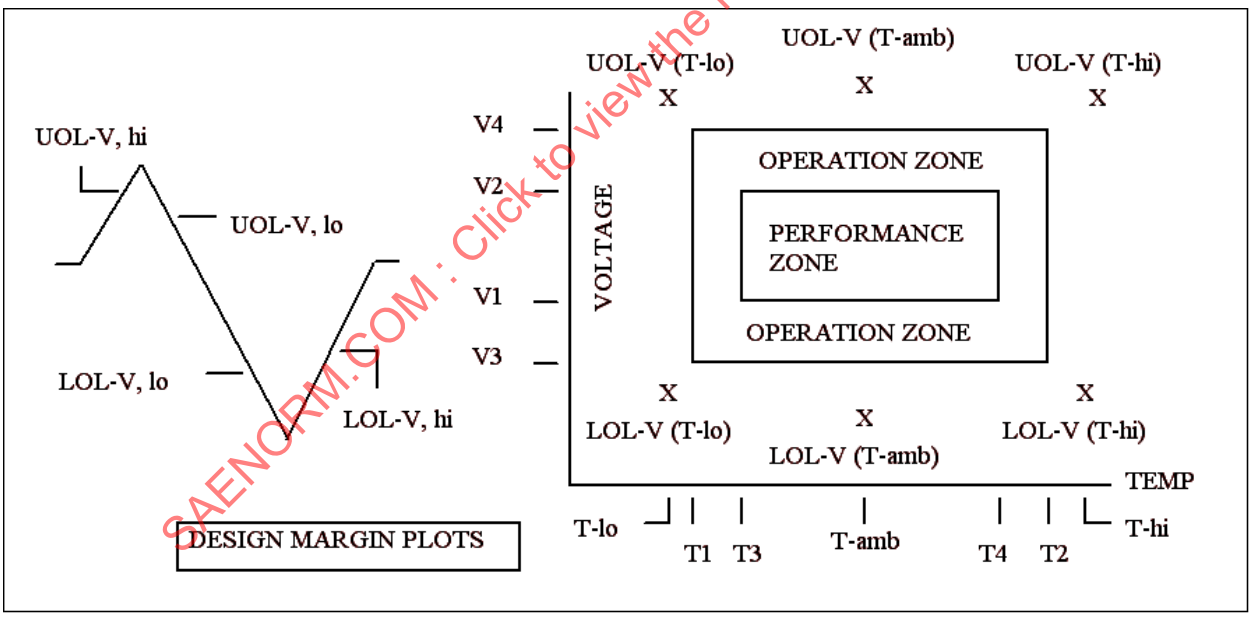

FIGURE 1 - DESIGN MARGINS PLOT - EXAMPLE

4.2 Voltage Interruptions-Transients

4.2.1 General

Although this section is presented separately, this testing can be combined with 4.1.

a. A key enabler is the “chattering relay” (Normally Closed relay contacts connected in series with the relay coil). It has the following properties:

- Creates randomness.
- Creates the actual complex mechanisms of the real event (e.g., contact arcing).
- Simple, low in cost.
- Makes it practical to be used in multi temperature testing.

b. R1-R2 simulate vehicle wiring inductance-resistance in the power and ground circuit and is important for developing voltage drops during transient conditions.

c. L1 simulates vehicle wiring inductance. R1 is to a degree redundant with L1.

d. L2 simulates vehicle inductive loads.

4.2.2 Power Cycle, Power Interruptions During Start-Up, Pulse F

The purpose of this test is to verify proper DUT start-up during ignition key-on (ignition switch or relay bounce) which can be severe over the full vehicle temperature range. This is especially important for verifying proper software initialization. It also addresses interruptions after start-up (e.g., poor connectors) in figure 2. Relay 1 provides the power on-off cycle and relay 3 is connected in a chattering configuration to provide the random noise representing contact bounce at power up and after. Figure 4 shows a typical example of the output from this circuit. This test applies to switched power and control circuits.

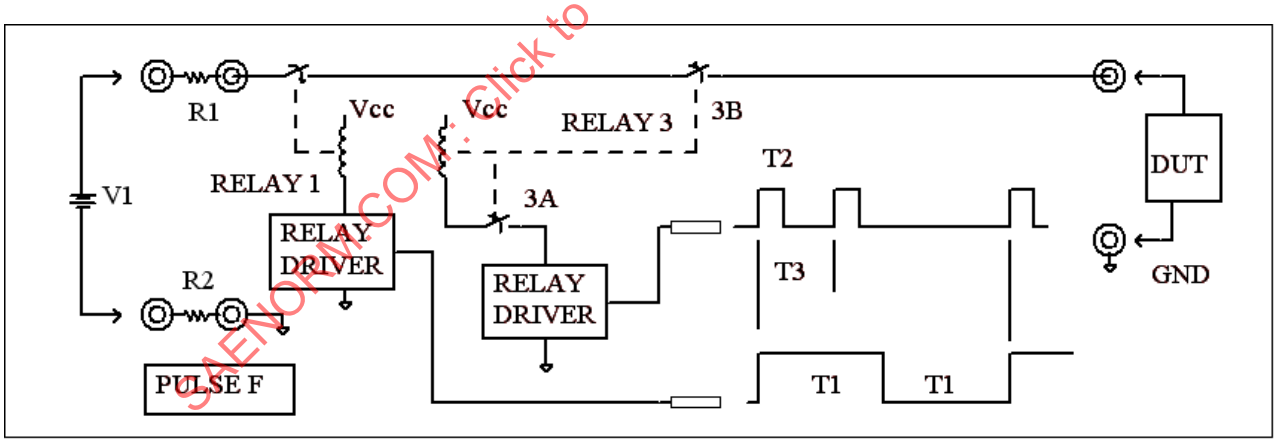

FIGURE 2 - TEST PULSE F SCHEMATIC

4.2.3 Inductive Transients - Pulse A1, A2, A1-a , A2-a, C

Historically ISO 7637-2 (reference 2.2.2) has been the standard for these types of vehicle transients but as reference 2.2.3 illustrates, this is not the case. The pulses in this document were developed to be a more realistic representation of actual vehicle transients. Figure 3 shows how they are generated.

Pulse A1 and A2 simulates the transients produced by switching off power to the DUT and an inductive load (L2) that is in parallel with the DUT. The pulse is produced at the start of period T1 when contact 3B opens. R3 provides adjustment of current through L2 to give different waveform characteristics (A1 = high current, A2 = low current). Figures 5 and 6 shows a typical example of the output from this circuit. This test applies to switched power and control circuits.

Pulse A1-a and A2-a are similar except that the opening of contact 3B is done by via a chattering relay to create a series of power interruptions during time T1 (also inductive transients due to L2). This simulates events due to intermittent connections - combination of contact fretting (corrosion) and vibration (e.g., hitting pothole) can cause such a connection (contributor to Trouble Not Indicated - TNI's).

Pulse C is produced by switching off an inductive load that shares a common power feed with the DUT. This is the same configuration as for pulse A1-a and A2-a except that the DUT connection point is different (power not removed from DUT). Figure 7 shows a typical example of the output from this circuit.

The main purpose of pulses A1, A1-a, A2 and A2-a is to observe if the DUT comes back to normal after the test (power is momentarily dropping out during the test). Pulse C should not affect normal operation. For all these transients, loading by the DUT will dramatically affect the waveshape (refer to reference 2.2.3 for technical discussion).

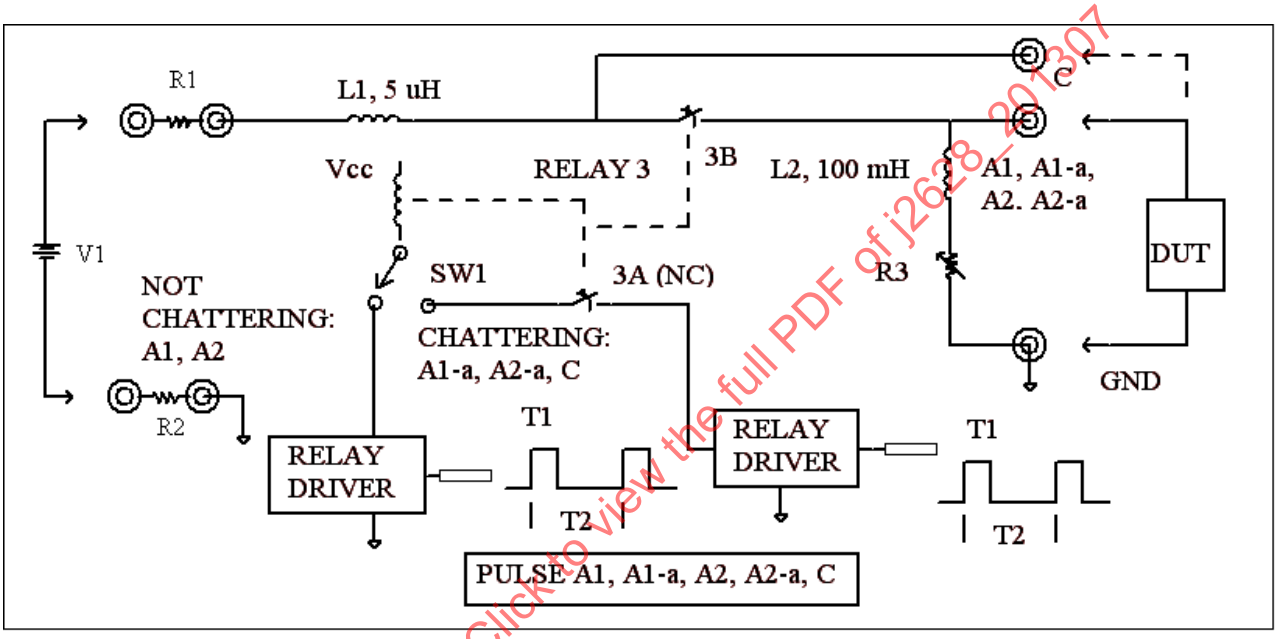

FIGURE 3 - PULSE A1, A2, A1-A, C SCHEMATIC

4.2.4 Voltage Interruptions-Transients Waveforms

The following waveforms are examples of the various tests. Each waveform will vary due to the randomness of mechanical contacts. Waveforms are open circuit, scale factors are per division.

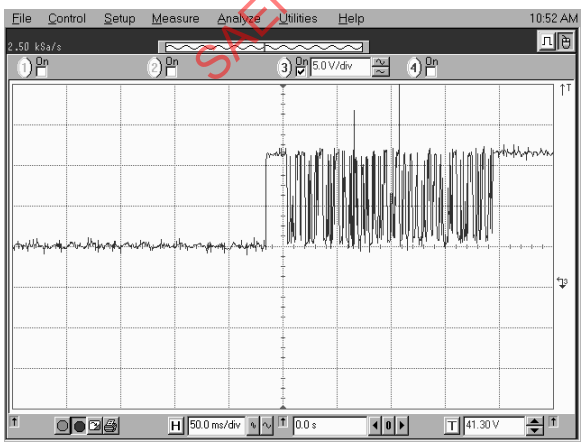

FIGURE 4 - EXAMPLE OF POWER INTERRUPTIONS AT START UP (50 ms, 5 V)

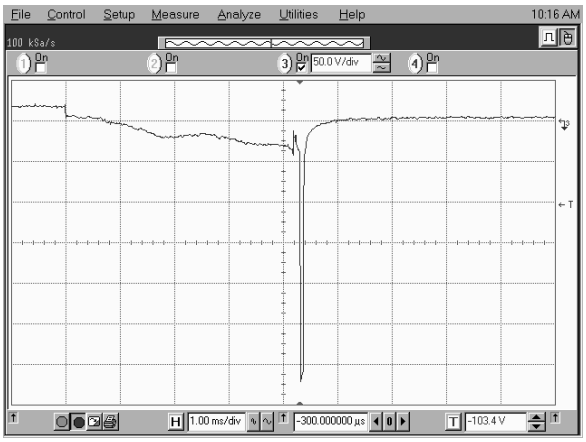

FIGURE 5 - EXAMPLE OF A1 (1 ms, 50 V)

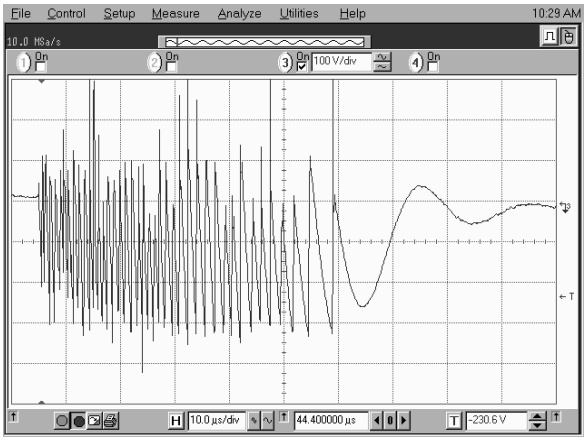

FIGURE 6 - EXAMPLE OF A2 (10 µs, 100 V)

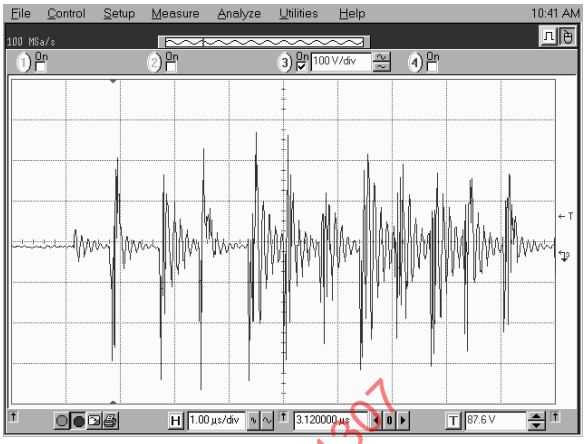

FIGURE 7 - EXAMPLE OF C (1 µs, 100 V)

4.3 Voltage Dropouts and Dips, See 2.2.4

This method verifies that a DUT is compatible with:

- Voltage Dropouts - high impedance (open circuit) typically due to poor connections (e.g., hitting pothole).
- Voltage Dips - low impedance most commonly experienced during engine starting. These dips can also occur as a result of a poor battery connection when a high current load is activated. Voltage dips can also be used to evaluate DUT voltage regulator input step response by monitoring the regulator output and looking for stability (limited overshoot, limited ringing).

Figure 8 shows the setup to generate these waveforms. The waveforms were not developed to accurately replicate actual vehicle waveforms but contain the elements necessary to identify DUT issues.

Other similar waveforms can be used. For these other waveforms, a faster rise and fall times may be needed which may require use of an electronic switch instead of the DC power amplifier.

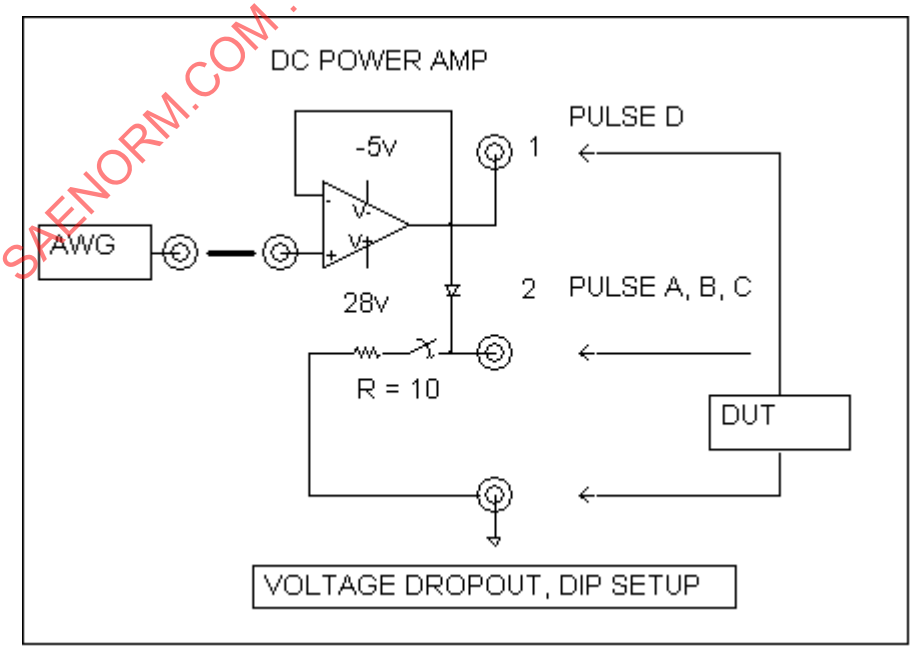

FIGURE 8 - VOLTAGE DROPOUT AND DIP SETUP

TABLE 1 - VOLTAGE DROP - DIP, PARAMETERS

Test	Level	Up, U1	T (1) (2)	Duration	Impedance	Acceptance Criteria
A	Fig 9	13.5	500µs, 5ms, 50ms	3 cycles 20 sec apart	High	II
B	Fig 10	13.5	Same as Test A	Same as Test A	High	II
C	Fig 11	13.5	500µs (single)	Same as Test A	High	I
D	Fig 12	13.5, 5.0	Same as Test A	Same as Test A	Low	II

1. Waveform transition time approximately 10µs.

2. Other values if concern to determine design margin. (see ref 2.2.4)

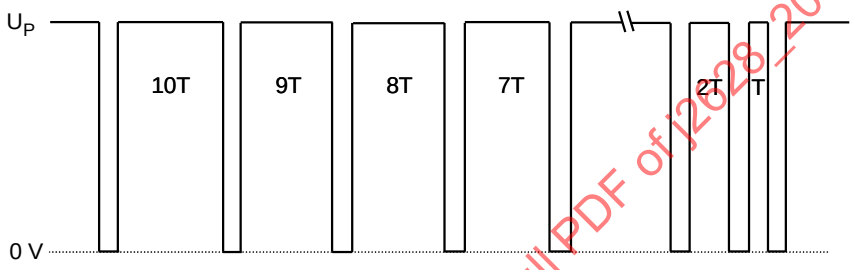

FIGURE 9 - VOLTAGE DROPOUT A

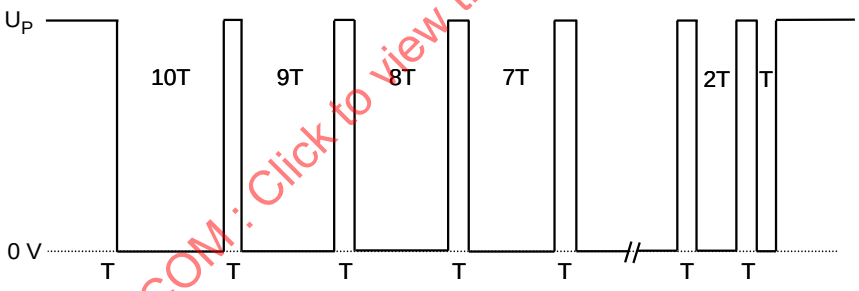

FIGURE 10 - VOLTAGE DROPOUT B

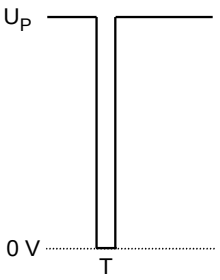

FIGURE 11 - VOLTAGE DROPOUT C

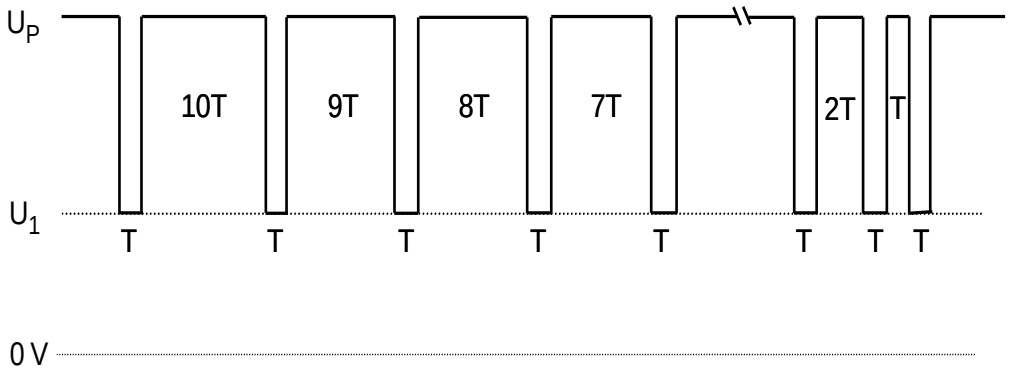

FIGURE 12 - VOLTAGE DIP D

4.4 Current Draw

This method verifies that the DUT draws expected currents under a number of conditions. It is a good indicator for a number of things such as DUT degradation during environmental testing, detection of inadvertent changes to the design or manufacturing process, detection of sneak paths. Since the current can have a complex waveform, it is important to use a true RMS current meter with sufficient frequency response and resolution. In addition, sufficient time should be allowed for currents to stabilize.

4.5 Switch Input Noise

This addresses the non ideal characteristics of module switch type inputs (e.g., power door locks, power windows). Figure 13 shows the simulator circuitry for this test method. It contains a chattering relay that is activated on the leading and trailing edge of switch SW1 on-off operation which represents switch bounce. The simulator also contains resistors (R1, R2) to reflect vehicle degradation (open = 50k ohms, closed = 50 ohms). Multiple channels are required to be activated individually or simultaneously.

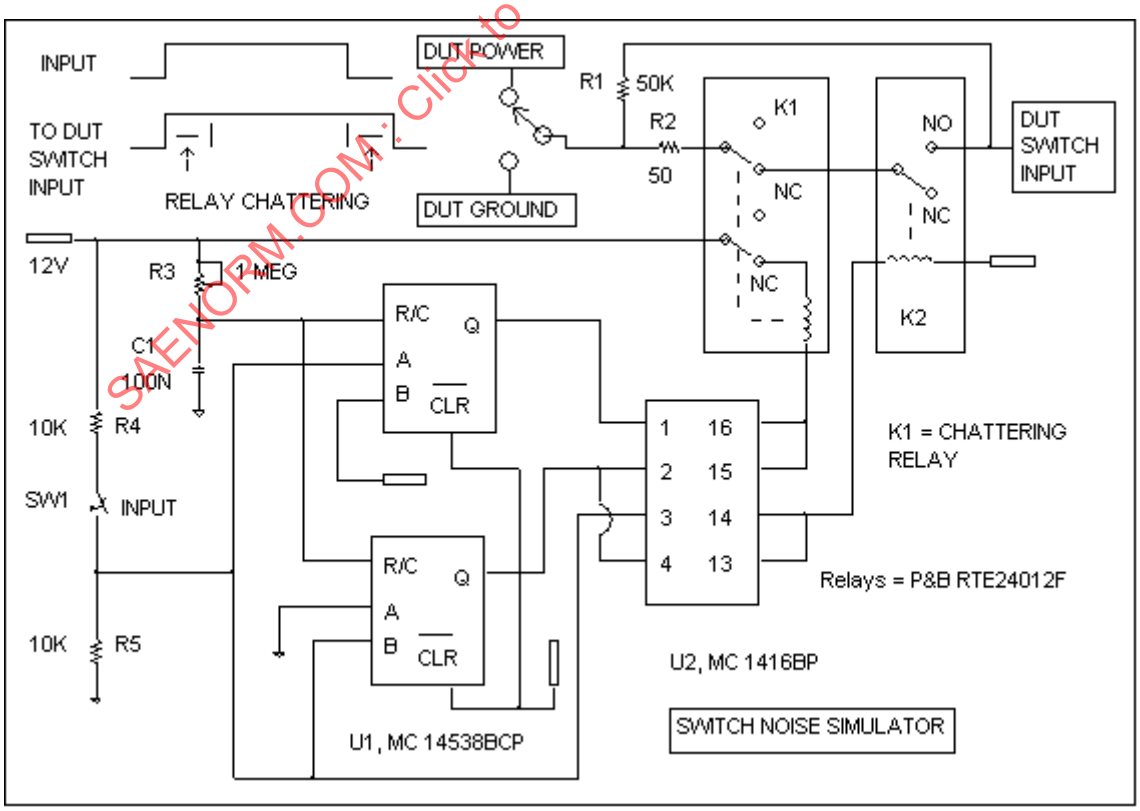

FIGURE 13 - SWITCH NOISE SIMULATOR

5. TEST EQUIPMENT

NOTE: Although separate circuits can be used for 5.1 to 5.4, Figure 14 shows an all-inclusive version - Product Assurance Robustness (PAR) Tester. The diagram shows 2 channels (AWG and DC Power Amp) which is useful for similar tests not mentioned in this document.

5.1 Transient Simulator Components

a. Relay 1: Controls power on-off.

b. Relay 2: Determines test configuration.

c. Relay 3: Chattering relay characteristics:

- Coil is 12 V AC (contains shading pole) operated at 12 V DC
- R = 20 ohms nominal, Inductance = 100-150 mH @ 60 Hz
- Contact rating = 10 amps (typical), DPDT
- Example, P&B KUP-14A15-12

d. R1, R2 Ground, Power Resistors: Default = 10 watt, 0.1 ohms, wire wound.

e. L1 Series Inductance: Nominal = 5 microhenry. Osborne Transformer 8745 or equivalent

f. L2 Inductive load used to create transients: Nominal = 100 mH, 1 ohm. Osborne Transformer 32416 or equivalent..

g. R3: Controls current through inductors. High current = 6 ohms (25 watt), Low current = 106 ohms (5 watt).

5.2 Arbitrary Waveform Generator

Able to create waveforms specified in this document.

5.3 DC Power Amplifier

DC-20 KHz (3 dB), Range = 0-24 volts, current capability consistent with DUT.

5.4 Switch Noise Simulator

See Figure 13, Multi-channel. Adjustable chattering time = 10-100 ms

5.5 Other Equipment

a. DUT exerciser-termination fixture. This provides DUT Input-Output terminations and a means of operating the DUT in its various modes.

b. Since interface compatibility is a major issue, the DUT should also be tested with other DUT's that it interfaces with. Configure so that it will fit into an environmental chamber (e.g., if too big to lay out flat on a breadboard, configure as stacked multiple smaller sub-breadboards). It should also allow injection of test signals. See Figure 15 for example.

c. Variable DC Power Supply - Capable of providing specified voltages at DUT current requirements. Shall not be affected by simulator (e.g., chattering relay noise).

d. Data Acquisition - Capable of monitoring the DUT signals and tracking when the DUT response exceeds predetermined limits.

e. Environmental Chamber - Capable of temp range required and nominal ramp rate of 3-5 °C per min.

f. True RMS current meter. Consistent with DUT frequency content and resolution requirements.

5.6 Test Equipment Tolerances - Characterization

Tolerances (unless otherwise specified): Voltage = ±0.5 volts, Current = 10 mA or 0.1 mA depending on test, Time-Resistance = ±10%, Temperature = ±2 °C

Even though some of these tests are intentionally random in nature (its real advantage) experience has shown that the DUT responses are very repeatable. The voltage waveforms produced should be periodically observed for degradation with an oscilloscope to verify correct waveform characteristics (many new scopes allow measurement of average and standard deviation). The amount of degradation over time is a function of the currents that the relay contacts must provide to the DUT and how much the relay is used.

Use reference 2.2.4 for transient characteristics. For the tests requiring use of the DC power amplifier, verify accuracy of the output waveforms both open circuit and loaded. The loaded waveforms should draw similar currents that the DUT would (default = 10 ohms). Maximum change from open circuit to loaded (amplitude, frequency response) = 10%.

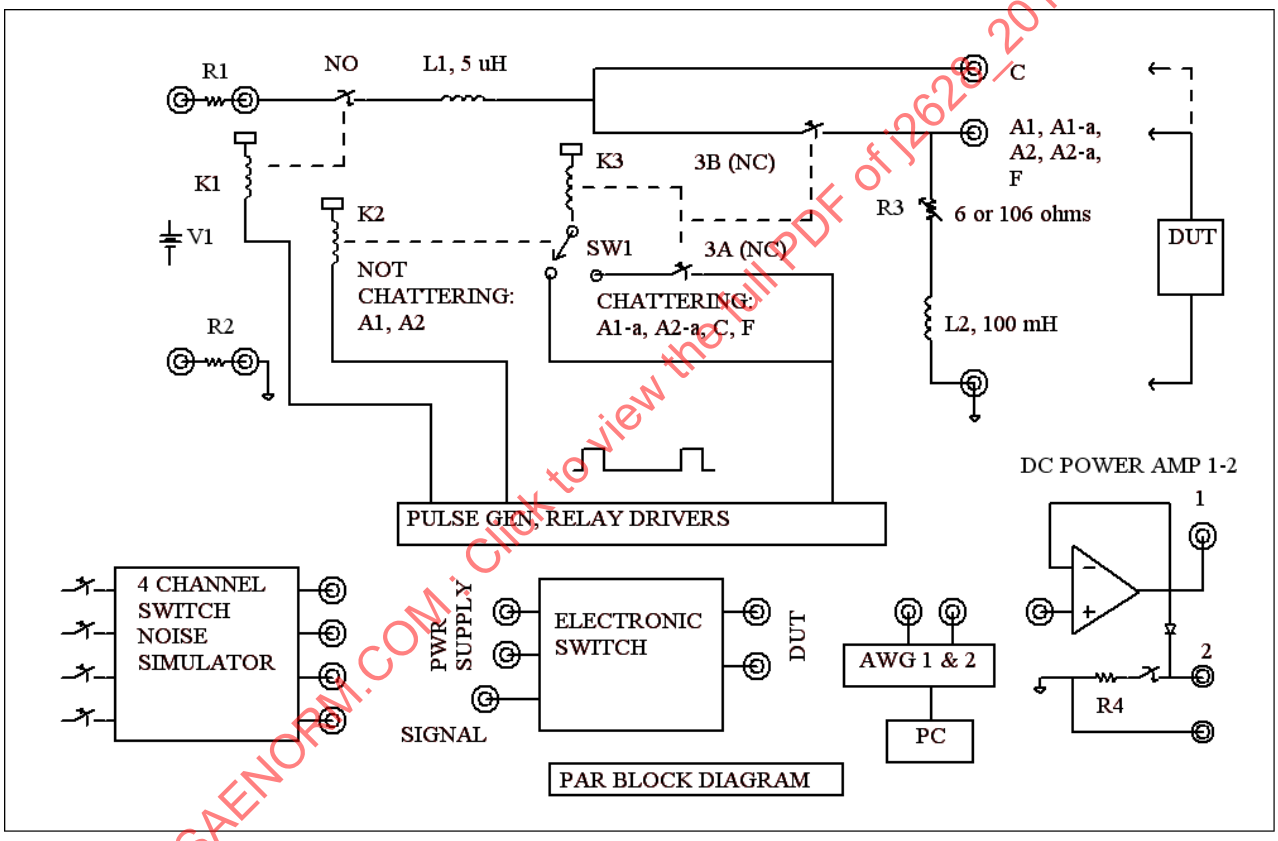

FIGURE 14, PAR TESTER

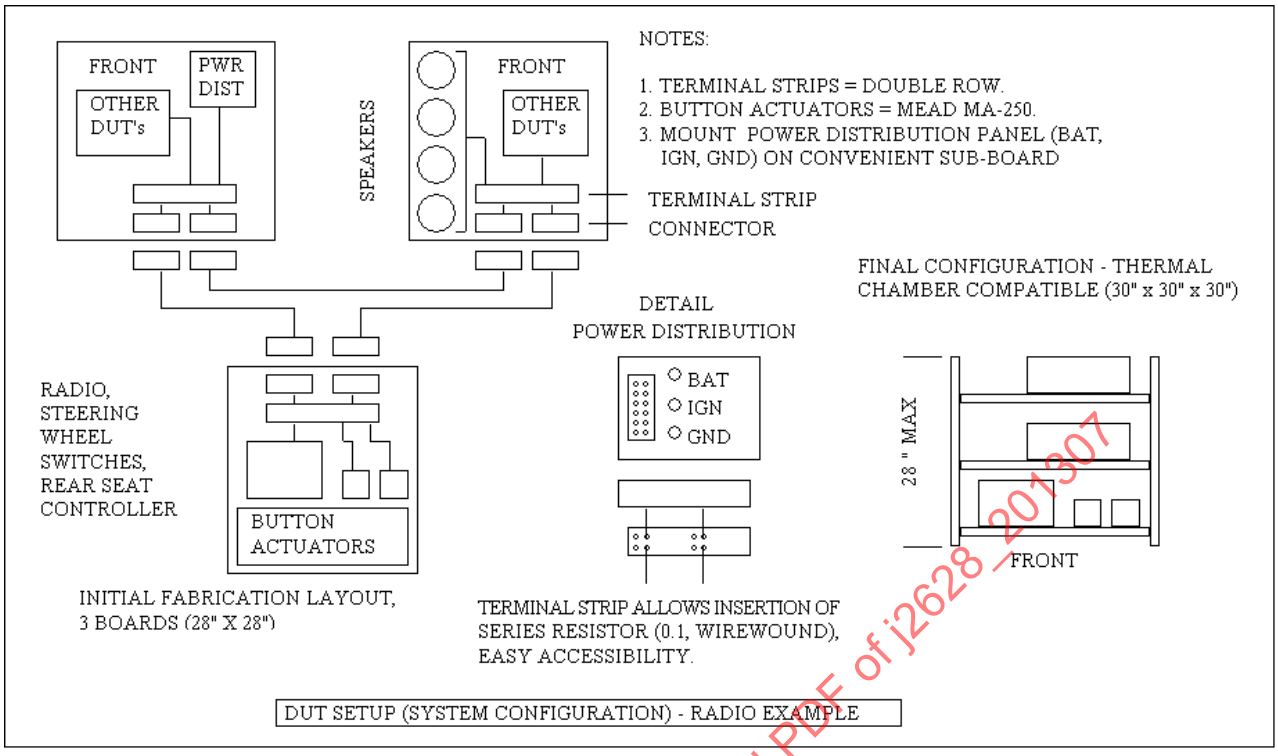

FIGURE 15 - DUT SETUP, SYSTEM CONFIGURATION

6. TEST PROCEDURES

6.1 General

a. Before a test plan is developed, the DUT shall undergo a Design Review by technical experts to determine where testing should be focused.

b. The DUT shall be connected to the actual operating devices (loads, sensors, etc.) using a test harness or the production wiring harness, as agreed upon between the vendor and the customer. If the original operating devices are not available, they may be simulated by methods outlined in SAE J1113-1.

c. For many of these methods, system and interface issues shall be addressed. Typical examples are:

- DUT output coil (e.g., solenoid) increase in resistance with temperature (may require placing load in thermal chamber with DUT).
- Wiring-connector resistance-inductance in ground and/or power circuits.
- DUT switch input resistance (default: closed switch = 50 ohms, open switch = 50k).

d. Due to R1 and R2, the voltage at the DUT may be different than the power supply voltage.

e. Place DUT in typical operating mode (most temp, voltage sensitive) and monitor key output signals.

f. For DUT's with communications bus, operate DUT in mode that creates near maximum bus activity. Note: Communications Bus analyzers can be sensitive to electrical noise and may need filtering or optical coupler.

g. If the DUT exhibits abnormal behavior during testing, monitor appropriate internal DUT signals to determine root cause (e.g., voltage regulator outputs, microprocessor resets).

6.2 Voltage-Temperature Design Margins

a. If practical, remove DUT temperature constraints to extend temp limits (e.g., instrument cluster plastic housing).

b. Determine applicable test method. Table 2 = More rigorous to determine design margin envelope. Table 3 = Abbreviated (e.g., Pre-Qual, Conformity) to verify at least a small design margin.

c. Resolution = 0.1 v.

TABLE 2 - EVALUATION METHOD A

Step	Action	Parameters	Result, Notes
	Ambient Temp		
1	Ramp voltage(1)	V-nom to 20 to 0 to V-nom, approx 10 V/min(2)	Predetermined response, No Lock-ups
2	Determine Voltage Limits		UOL-V (T-amb), hi/lo LOL-V (T-amb), lo/hi
3	Apply Voltage Interruptions, Transients.	(3)	(3)
	Low Temp		
4	Lower temp, power on	T3 – 5 °C, V-nom	Note DUT operation during temp transition
5	Turn power off	10 min	Temp soak
6	Power on	V-nom	Verify proper DUT start-up.
7	Repeat voltage ramp and determine limits.		UOL-V (T3 – 5 °C), hi/lo LOL-V (T3 – 5 °C), lo/hi
8	Repeat Step 3.	T3 – 5 °C	
9	Step to lower temp with power on	T3 – 10 °C, V-nom	
10	Turn power off	10 min	Temp soak
11	Power on	V-nom	Verify proper DUT start-up.
12	Repeat steps 9-11 until low temp limit found (Steps = 5 °C, limit to 15 °C beyond spec).	LOL-T (V-nom)	
13	Compute T-lo = LOL-T (V-nom) + 5 C		T-lo
14	Repeat voltage ramp and determine limits.	T-lo	UOL-V (T-lo), hi/lo LOL-V (T-lo), lo/hi
	High Temp		
15	Increase temp, power on	T4 + 5 °C, V-nom	Note DUT operation during temp transition
16	Turn power off	10 min	Temp soak
17	Power on	10 min, V-nom	Verify proper DUT start-up.
18	Repeat voltage ramp and determine limits.		UOL-V (T4 + 5 °C), hi/lo LOL-V (T4 + 5 °C), lo/hi
19	Repeat Step 3.	T4 + 5 °C	
20	Step to next higher temp with power on	T4 + 10 °C, V-nom	
21	Turn power off	10 min	Temp soak
22	Power on	10 min, V-nom	Verify proper DUT start-up.
23	Repeat steps 20-22 until high temp limit found (Steps = 5 °C, limit to 15 °C beyond spec).	UOL-T (V-nom)	
24	Compute T-hi = UOL-T (V-nom) - 5 °C		T-hi
25	Repeat voltage ramp and determine limits.	T-hi	UOL-V (T-hi), hi/lo LOL-V (T-hi), lo/hi

1. Ramp must be linear, not course digital steps. If applicable, connect Battery and Ignition inputs together.
2. 20 volts is considered reasonable upper limit. The only DC voltage higher than 20 volts in a vehicle is double voltage jump start (24 volts).
3. Recommended tests: Section 6.3, pulses F and A1-a.

TABLE 3 - EVALUATION METHOD B (ABBREVIATED VERSION OF METHOD A)

Step	Action	Parameters	Result, Notes
	Ambient Temp		
1	Ramp voltage(1)	V-nom to 20 to 0 to V-nom, approx 10 V/min(2)	Predetermined response, No Lock-ups
2	Determine Voltage Limits		UOL-V (T-amb), hi/lo LOL-V (T-amb), lo/hi
3	Apply Voltage Interruptions, Transients.	(3)	(3)
	Low Temp		
4	Lower temp, power on	T3 – 5 °C, V-nom	Note DUT operation during temp transition
5	Turn power off	10 min	Temp soak
6	Power on	V-nom	Verify proper DUT start-up.
7	Repeat voltage ramp and determine limits.		UOL-V (T3 - 5 °C), hi/lo LOL-V (T3 - 5°C), lo/hi
8	Repeat Step 3	T3 – 5 °C	
	High Temp		
10	Increase temp, power on	T4 + 5 °C, V-nom	Note DUT operation during temp transition
11	Turn power off	10 min	Temp soak
12	Power on	10 min, V-nom	Verify proper DUT start-up.
13	Repeat voltage ramp and determine limits.		UOL-V (T4 + 5 °C), hi/lo LOL-V (T4 + 5 °C), lo/hi
14	Repeat Step 3.	T4 + 5 °C	

1. Ramp must be linear, not course digital steps. If applicable, connect Battery and Ignition inputs together.
2. 20 volts is considered reasonable upper limit. The only DC voltage higher than 20 volts in a vehicle is double voltage jump start (24 volts).
3. Recommended tests: Section 6.3, pulses F and A1-a.

6.3 Voltage Interruptions, Transients

This section gives details for generating electrical noise either as a separate test or as part of another test (e.g., 6.2.).

Connect simulator to applicable inputs of DUT. Apply tests per Table 4 and verify DUT response per Acceptance Criteria.

NOTE: Ensure that Power Supply and DUT active terminations (e.g., signal generators) are not affected by simulator (e.g., chattering relay noise).