IEC TS 62607-6-16

Edition 1.0 2022-11

TECHNICAL SPECIFICATION

colour inside

Nanomanufacturing – Key control characteristics – Part 6-16: Two-dimensional materials – Carrier concentration: Field effect transistor method

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NANOMANUFACTURING – KEY CONTROL CHARACTERISTICS –

Part 6-16: Two-dimensional materials – Carrier concentration: Field effect transistor method

FOREWORD

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The text of this Technical Specification is based on the following documents:

Draft	Report on voting
113/679/DTS	113/698/RVDTS

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC TS 62607 series, published under the general title *Nanomanufacturing – Key control characteristics*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

Atomically thin 2D materials are expected to be used for future electrical sub-systems or electronic device applications. For these applications, the materials need to be doped with dopants to generate carriers. In contrast to 3D bulk materials, carrier concentrations in 2D materials are difficult to measure directly due to their limited thickness.

– Different from conventional 3D bulk materials in which doping effect is induced from activation of substitutional dopant atoms, the doping effect in 2D materials is mostly induced by generation of free carriers, for example electrons by using plasma treatment, chemical treatment, etc.

– In the 3D bulk materials, carrier concentration can be obtained by measuring concentration of dopant atoms under the assumption that both concentrations are the same. Therefore, it is possible to measure the doping concentration in 3D bulk materials using secondary ion mass spectroscopy (SIMS), which measures the concentration of dopant atoms, and using I-V or C-V characterization, which measures the concentration of free charge carriers such as electrons and holes [1][1].

– In contrast, in the 2D materials, carrier concentration needs to be measured for carriers such as electrons and holes which are induced from external means such as plasma treatment or chemical treatment.

For this reason, a standard method to determine the carrier concentration needs to be established for 2D materials.

[1] Numbers in square brackets refer to the Bibliography.

NANOMANUFACTURING – KEY CONTROL CHARACTERISTICS –

Part 6-16: Two-dimensional materials – Carrier concentration: Field effect transistor method

1 Scope

This part of IEC TS 62607 establishes a standardized method to determine the key control characteristic

- carrier concentration

for semiconducting two-dimensional materials by the

- field effect transistor (FET) method.

For semiconducting two-dimensional materials, the carrier concentration is evaluated using a field effect transistor (FET) test by a measurement of the voltage shift obtained from transfer curve upon doping process. The FET test structure consists of three terminals of source, drain, and gate where voltage is applied to induce the transistor action. Transfer curves are obtained by measuring drain current while applying varied gate voltage and constant drain voltage with respect to the source which is grounded.

- The method is applicable to semiconducting two-dimensional materials with a bandgap like that in transition metal dichalcogenides (MoS_2, $MoTe_2$, WS_2, WSe_2, etc.) and black phosphorous. Pristine graphene shows semi-metallic characteristics without bandgap, and therefore this method is not applicable to pristine graphene. However, it can be used for other graphenes with bandgap (for example, semiconducting graphene oxide).
- It is likely that the measurement results will help to qualify technologies if they are usable for future electrical sub-systems or electronic device applications.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1 General terms

3.1.1
key control characteristic
KCC
key performance indicator
material property or intermediate product characteristic which can affect safety or compliance with regulations, fit, function, performance, quality, reliability or subsequent processing of the final product

Note 1 to entry: The measurement of a key control characteristic is described in a standardized measurement procedure with known accuracy and precision.

Note 2 to entry: It is possible to define more than one measurement method for a key control characteristic if the correlation of the results is well-defined and known.

3.1.2
bilayer graphene
2LG
two-dimensional material consisting of two well-defined stacked graphene layers

Note 1 to entry: If the stacking registry is known, it can be specified separately, for example, as "Bernal stacked bilayer graphene".

[SOURCE: ISO/TS 80004-13:2017 [2], 3.1.2.6]

3.1.3
few-layer graphene
FLG
two-dimensional material consisting of three to ten well-defined stacked graphene layers

[SOURCE: ISO/TS 80004-13:2017 [2], 3.1.2.10]

3.1.4
two-dimensional material
2D material
material, consisting of one or several layers with the atoms in each layer strongly bonded to neighbouring atoms in the same layer, which has one dimension, its thickness, in the nanoscale or smaller, and the other two dimensions generally at larger scales

Note 1 to entry: The number of layers when a two-dimensional material becomes a bulk material varies depending on both the material being measured and its properties. In the case of graphene layers, it is a two-dimensional material up to ten layers thick for electrical measurements, beyond which the electrical properties of the material are not distinct from those for the bulk (also known as graphite).

Note 2 to entry: Interlayer bonding is distinct from and weaker than intralayer bonding.

Note 3 to entry: Each layer may contain more than one element.

Note 4 to entry: A two-dimensional material can be a nanoplate.

[SOURCE ISO/TS 80004-13:2017 [2], 3.1.1.1]

3.2 Key control characteristics measured in accordance with this document

3.2.1
2D carrier concentration
characteristic described by the areal density of electrons or holes free to move in two dimensions due to the atomical thinness of 2D materials that restricts the movement of the carriers in the third direction

Note 1 to entry: The unit of 2D carrier concentration is [cm^{-2}]

Note 2 to entry: In general, increased doping leads to increased conductivity due to the higher concentration of the charge carriers. Carrier density in conventional semiconductors is usually tuned with substitutional doping. However, substitutional doping is very difficult in 2D materials due to their nanometre-scale thickness. Generally, in conventional semiconductors, the doping concentration at room temperature is assumed to be the same as the free carrier concentration because free carriers such as electrons or holes are generated from fully ionized dopant atoms. Therefore, doping concentration in bulk semiconductors can be estimated by various methods, e.g. SIMS, X-ray photoelectron spectroscopy (XPS), and I−V (C−V) characterization. By contrast, doping in 2D materials is induced mainly by electrostatic gating or charge transfer and therefore doping concentration in 2D materials needs to be determined by electrical characterization. [3]

3.3 Terms related to the measurement method

3.3.1
field effect transistor
FET
transistor in which the voltage on one terminal (gate) creates a field that allows or disallows conduction between the other two terminals (source and drain)

Note 1 to entry: The carrier concentration of a semiconductor can be modulated by electrostatic gating in an FET configuration. In the FET, two metal electrodes (source and drain, S/D) formed on the sample are used to provide driving force for the lateral current conduction, while the third electrode (gate, G) is used to modulate the current conduction on the sample surface across a gate dielectric material.

3.3.2
transfer curve
graph that provides corresponding output current values for each possible voltage input to an electronic or control system component

Note 1 to entry: Transfer curves are obtained by measuring drain current (I_D) as a function of gate voltage (V_G) at constant drain voltage (V_D).

3.3.3
charge neutral point
point at which the electron current is equal to hole current in semiconductors

4 General

4.1 Measurement principle

Doping concentration, which is equivalent to free carrier concentration, can be determined by shift of charge neutral point in transfer curves (drain current as a function of gate voltage). This method requires to use a transistor, more specifically a FET, and works well for semiconducting materials.

4.2 Sample preparation method

4.2.1 Sample preparation

2D materials, which are obtained mostly through micromechanical exfoliation or chemical vapour deposition, are typically deposited on Si substrates covered with thermally grown SiO_2 film. Raman spectroscopy and XPS can be performed to identify their chemical components and to analyse defects. Heterostructure is prepared by stacking 2D materials.

4.2.2 Fabrication of FET

A typical example for substrates to be used for 2D materials is

- silica on silicon (SiO_2 on Si).

The bottom gate electrode can consist of

- highly doped Si substrate wafers used for electrical back gating, underneath the SiO_2.

The bottom gate-dielectric layer can consist of

- typical values of 90 nm and 285 nm thick SiO_2 layer.

The semiconducting layer can consist of

- 2D materials, e.g. graphene, MoS_2, $MoTe_2$, WSe_2, WS_2, black phosphorus.

The top source and drain electrode materials can consist of

- stable metals with low resistivity, e.g. Au, Ag, and adhesion metals, e.g. Ti, Cr, with the total thickness of metal electrodes in the range of 5 nm to 50 nm.

The channel length between source and drain electrodes distance is

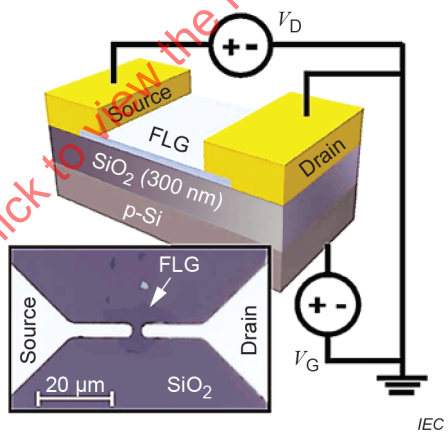
- the distance between source and drain typically in the range of 100 nm to 10 µm, with the patterning process of the electrodes that can be done by optical lithography or electron-beam lithography.

The encapsulation of the sample can be adopted for the following reason.

- 2D materials carrier concentration can be affected by the surface conditions. But the encapsulation effect is not quantified and the encapsulation procedures are not considered in this document.

The fabricated sample's baseline condition for electrically working before the measurement.

- It is recommended to maintain gate leakage current measured from tested devices less than 10^{-10} A.

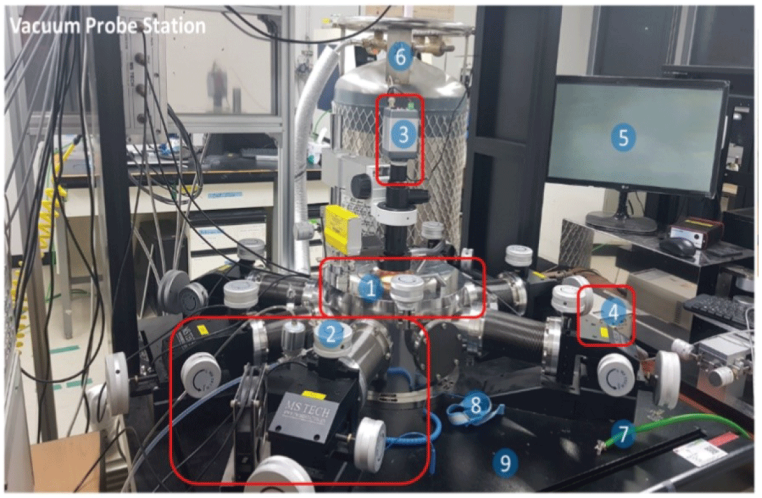


SOURCE: Reproduced from Y. Lim et al. (2012) [4], with the permission of American Chemical Society.

Figure 1 – Schematic of a back-gated graphene FET (inset: top view of the optical microscopic image)

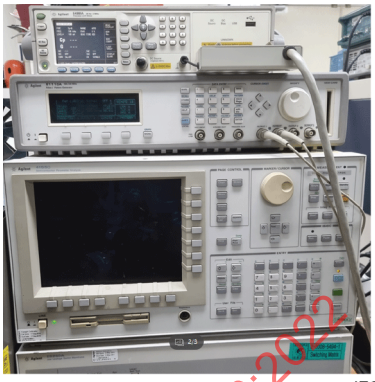
4.3 Description of measurement equipment

Electrical properties of fabricated FET devices are measured with a semiconductor parameter analyser, as shown in Figure 2 b). The vacuum probe station (Figure 2 a)) is used to obtain more accurate results with minimal effects of surface contamination.



IEC

a) Vacuum probe station



IEC

b) Semiconductor parameter analyser

IEC

c) Temperature controller

Key

1 Vacuum chamber
2 Probe position manipulator
3 CCD camera
4 Light bank of CCD
5 Computer
6 Liquid N_2 cylinder
7 Machine grounding
8 Human grounding bracelet
9 Anti-vibration table

Figure 2 – Experimental setup for measurements of electrical properties of FET device

The analyser typically is connected to a probe station, as shown in Figure 2. For more detailed measurements of electrical properties, a temperature-dependent test can be performed. For example, the temperature inside the probe station is controlled by a heater for heating and liquid N_2 source for cooling. Before electrical measurements, the equipment, the device under test, and any electrically conducting media such as tweezer and human-being shall be properly grounded to avoid the damage on sample due to the electrostatic discharge. The schematic of graphene FET device under test and the top view of the sample are as in Figure 1.

4.4 Ambient conditions during measurement

The device under test shall be placed and probed inside a vacuum chamber as shown in Figure 2 a). Because 2D materials are air and moisture sensitive, the measurement can be performed in the vacuum chamber with a controlled pressure level. The measurement is carried out after the pressure of the chamber is lowered below 4 Pa, which is equivalent to about 30 mTorr.

5 Measurement procedure

5.1 Calibration of measurement equipment

Calibration and adjustments shall be performed periodically so that the instruments satisfy the measurement specifications. For typical semiconductor parameter analysers, it is recommended to perform the calibration once a year.

5.2 Detailed protocol of the measurement procedure

The carrier concentration measurement of the 2D materials needs to be conducted in the following procedure.

1) When preparing the measurement by using a probe station, make sure that three probes are electrically contacted to the three terminals (source, drain, and gate electrodes) of the loaded sample inside the vacuum chamber.
2) Pump down the probe station chamber to the required vacuum level.
3) Then, initiate a scan; with varying gate voltage, current flow is measured between source and drain terminals of the sample.
4) Obtain a plot of drain current as a function of gate voltage.
5) Purge the probe station chamber, then remove the sample from the chamber.

6 Data analysis and interpretation of results

6.1 General

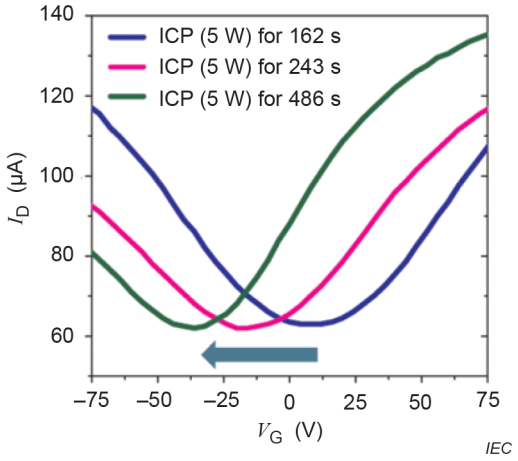
In the FET configuration, the charge carrier concentration above the threshold voltage (V_{th}) to turn on channel conduction can be estimated by $n = C_{ox}(V_G - V_{th})/e$, where n is the carrier concentration of 2D semiconducting material, C_{ox} is the capacitance of a dielectric material which is usually oxide, V_G is the gate voltage applied, and e is the electronic charge ($1{,}6 \times 10^{-19}$ C). Alternatively, the carrier concentration is estimated by $n = C_{ox}\Delta V / e$, where ΔV is the voltage shift. ΔV from transfer curves is determined by various methods. Table 1 summarizes the corresponding specification of key control characteristics.

Table 1 – Specification of key control characteristics, 2D carrier concentration

Item No.	Item	Specification	Unit	Measurement method	Standard
1-1	2D carrier concentration	Nominal [ ] ± Tolerance [ ]	cm^{-2}	Voltage shift (ΔV) obtained from transfer curves of FET	N/A

6.2 When the minimum conductance neutral point is clear

In the case where the minimum conductance neutral point is clear (e.g. Dirac point from graphene FETs), the voltage shift (ΔV) of the neutral point is used to determine the carrier concentration (See Figure 3).



Key

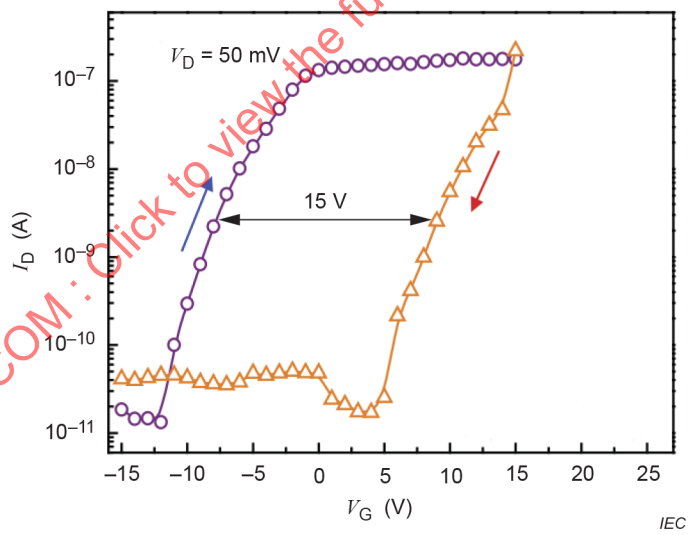
ICP inductively coupled plasma

SOURCE: Reproduced from Y. Lim et al. (2012) [4], with the permission of American Chemical Society.

Figure 3 – Voltage shift obtained from transfer curves upon plasma doping with various plasma treatments onto the graphene, using 300-nm-thick SiO_2 back gate insulator

6.3 When the minimum conductance neutral point is unclear

In the case where the minimum conductance neutral point is unclear, the parallel voltage shift between the points in I-V curves is used to determine the carrier concentration (See Figure 4).



SOURCE: Reproduced from M. S. Choi et al. (2013) [5], with the permission of Springer Nature.

Figure 4 – Voltage shift obtained from transfer curves of MoS_2 FET

7 Results to be reported

7.1 Cover sheet

The results of the measurement shall be documented in a measurement report, including the date and time of the measurement as well as the name and signature of the person responsible for the accuracy of the report.

7.2 Product or sample identification

The report shall contain all information to identify the test sample and trace back the history of the sample.

- General procurement information, in accordance with the relevant blank detail specification.
- General material description in accordance with the relevant blank detail specification, including a technical drawing:
  - top view, indicating the inspected area and location of the measurement positions;
  - cross section, showing the layer structure.

NOTE A blank detail specification for graphene is under development (IEC 62565-3-1).

7.3 Measurement conditions

The testing chamber and the laboratory ambient conditions during the test.

- Testing chamber baseline vacuum pressure level: 0,1 mPa < p < 30 mPa.
- Testing chamber temperature range: 15 °C < T < 25 °C.
- Testing chamber lighting condition: the-turned-off-lighting.
- Laboratory ambient temperature range: 15 °C < T < 25 °C.
- Range of the laboratory ambient relative humidity: 20 % < RH < 70 %.

7.4 Measurement specific information

- The method shall be described, including a drawing or photograph of the system.
- All the measurement equipment shall be calibrated.
- Values of quantities (carrier concentration n, or gate voltage V and drain current I, if applicable) to obtain the mean value and its standard deviation, number of measurements, resolution, linearity and accuracy of all involved instruments.

7.5 Measurement results

- Sampling plan used: A number of sample devices shall be fabricated by one batch of the same process and be provided for the measurement. Metallic electrodes onto the 2D materials can show a variance of electrical contact resistance which is dependent upon the different plasma treatment conditions defined in IEC TS 62607-6-5. [6]
- Table of mean values and standard deviation of carrier concentration for the sample devices defined in the sampling plan.
- Maps for carrier concentration and optionally dopant concentration.
- The experimentally measured results obtained from Graphene FET, Graphene/hBN/MoS_2 FET, $MoTe_2$ FET, and WSe_2 FET are shown in Annex A, Annex B, Annex C, and Annex D, respectively.

Annex A
(informative)

Graphene FET

A.1 Background

To obtain carrier concentration of graphene, two probe (source and drain electrodes) electrical measurements are performed. As in Figure 3, the transfer curves of a graphene FET are plotted, then the charge neutral points are extracted from transfer curves and the minimum points of the curves.

Figure 3 shows the transfer characteristics (drain current as a function of gate voltage, I_D-V_G) obtained after doping-inducing Ar plasma treatment for the graphene FET for treatment times of 162 s, 243 s, and 486 s. Here, the voltage shifts between charge neutral points extracted from several transfer curves are observed, due to the Ar plasma treatment of different conditions.

Neutral voltage point (V_{np}) is 8 V for 162 s of treatment, 18 V for 243 s, and 37 V for 486 s. Carrier concentration was calculated from $n = C_{ox}\Delta V / e$, where C_{ox} is $\varepsilon_0 \varepsilon_{SiO_2} / t_{SiO_2} = 1{,}15 \times 10 - 8\, F / \mathrm{cm}^2$. See Table A.1 for calculated results, where additional treatment times from 162 s were used to measure voltage shift ΔV.

A.2 Test report

According to the observed voltage shift in the graphene-FET, 2D carrier concentration in the charge storage layer can be calculated from $n = C_{ox}\Delta V / e$. The results are shown in Table A.1.

Table A.1 – 2D carrier concentration measured from graphene-FET for different doping-inducing Ar plasma treatment times

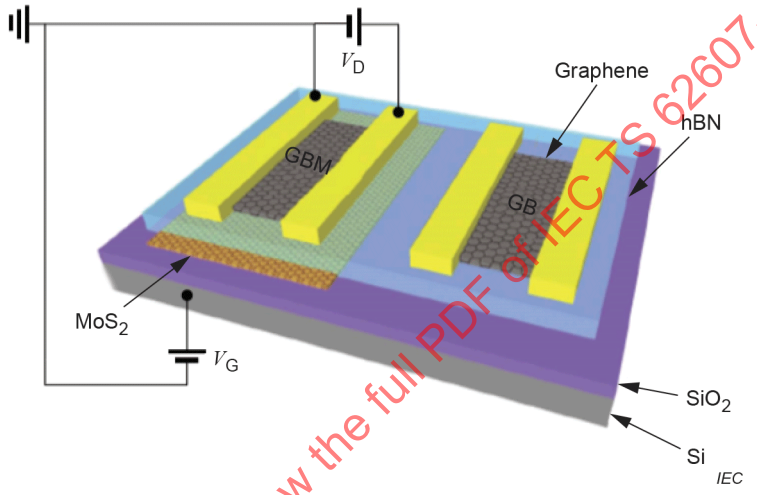
Additional Ar plasma treatment time (s) compared to the baseline of 162 s.	Voltage shift (V)	Carrier concentration (cm^{-2})
81 (= 243 s − 162 s)	10	$7{,}20 \times 10^{11}$
324 (= 486 s − 162 s)	29	$2{,}08 \times 10^{12}$

Annex B
(informative)

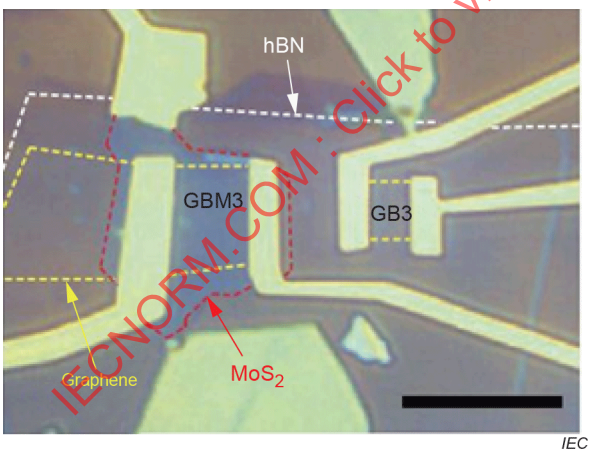
Graphene/hBN/MoS_2 heterostructure memory FET

B.1 Background

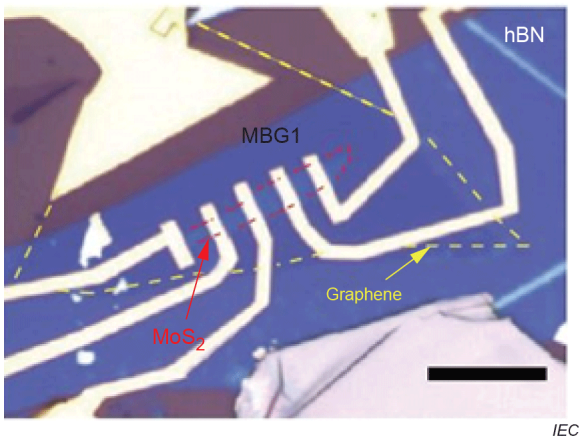
To obtain stored carrier concentration in graphene or 2D MoS_2 in heterostructure memory FETs, two probe electrical measurements are performed. A schematic view of a representative device and optical microscopic pictures of various memory device schemes are illustrated in Figure B.1. Transfer curves of the memory FET are plotted, as shown in Figure B.2. [5] Voltage differences between forward and reverse sweeps are observed from the transfer curves, which are attributed to charge storing into and releasing from a 2D layer.



(a) Schematic view and circuit diagram of heterostructured FET



(b) GBM device fabricated (scale bar, 10 µm)



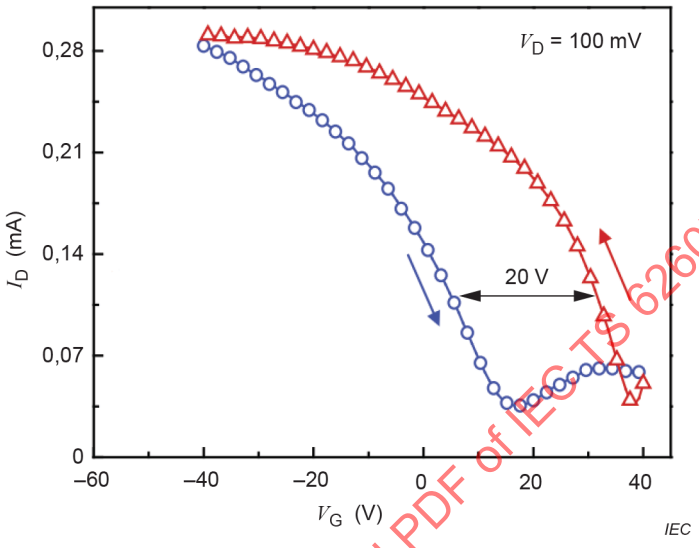
(c) MBG device fabricated (scale bar, 10 µm)

NOTE The devices in (b) and (c) are denoted as GBM3 and MBG1, respectively [4]. The dotted lines indicate the boundaries of each 2D material. G, B, and M represent graphene, hexagonal boron nitride (hBN), and molybdenum disulphide (MoS_2), respectively. In (b), the device denoted as GBM consists of graphene as the FET channel, hBN as the tunnel barrier and MoS_2 as the charge trapping layer. In (c), the device denoted as MBG consists of MoS_2 as the FET channel, hBN as the tunnel barrier and graphene as the charge trapping layer. These two types of heterostructured channel give tunnelling devices of different FET characteristics.

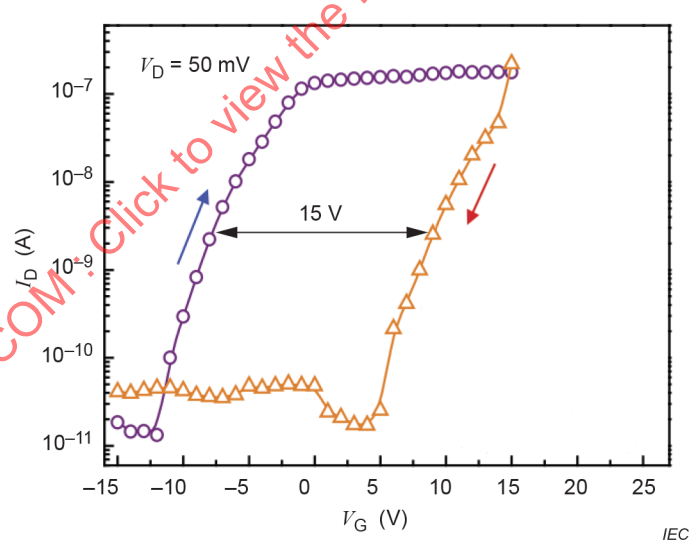
SOURCE: Reproduced from M. S. Choi et al. (2013) [5], with the permission of Springer Nature.

Figure B.1 – Heterostructure FETs: (a) schematic view and circuit diagram of the fabricated device; (b) optical microscopic photograph of GBM FET; (c) optical microscopic photograph of MBG FET

For GBM devices, thin layers of MoS_2 were mechanically exfoliated on a silicon wafer with 280-nm-thick SiO_2. After hBN and graphene were exfoliated onto wafers coated with polymethyl methacrylate (PMMA) and a thin release layer, PMMA film was removed from the wafer. Then, hBN and graphene were sequentially transferred onto the wafer containing the MoS_2. MBG devices were fabricated by a similar method, in a reverse-stacking order. Source and drain electrodes were formed through electron-beam lithography (EBL) and deposition of Cr/Pd/Au (1 nm/10 nm/50 nm) for GBM and Ti/Au (0,5 nm/50 nm) for MBG, where the doped Si substrate underneath the SiO_2 layer was used as a back gate.



(a) Voltage shift of GBM FET transfer curve



(b) Voltage shift of MBG FET transfer curve

SOURCE: Reproduced from M. S. Choi et al. (2013) [5], with the permission of Springer Nature.

Figure B.2 – Voltage shift obtained from transfer curves of two types of memory device upon charge injection

B.2 Test report

According to the observed voltage shift in the hetero-structure memory devices, 2D carrier concentration in the charge storage layer can be calculated from $n = C_{ox}\Delta V / e$. The results are shown in Table B.1.

Table B.1 – Carrier concentration derived from the electrical characteristics of GBM and MBG

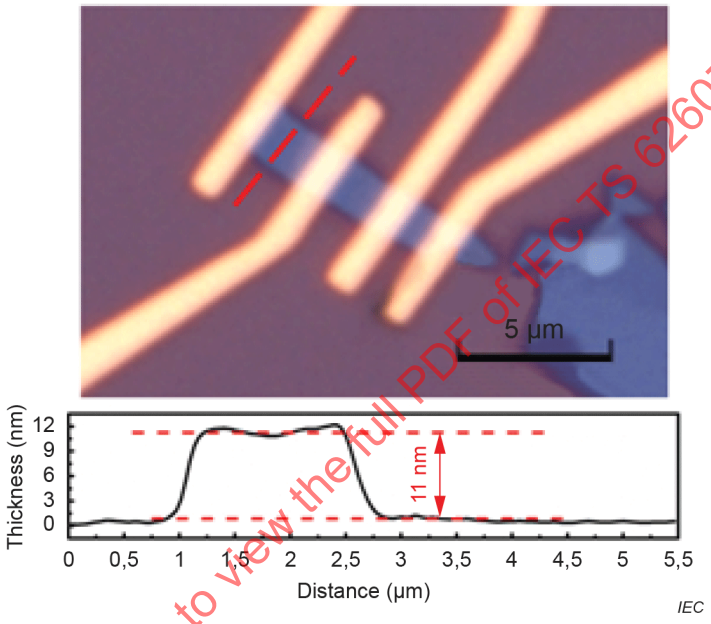
Structure	**Voltage shift** (V)	**Carrier concentration** (cm^{-2})
GBM	20	$1{,}50 \times 10^{12}$
MBG	15	$1{,}13 \times 10^{12}$

Annex C
(informative)

$MoTe_2$ FET

C.1 Background

To obtain stored carrier concentration in 2D $MoTe_2$ FETs, four probe electrical measurements are performed. Optical microscopic pictures of 2D $MoTe_2$ FETs are shown in Figure C.1. Transfer curves of FET are plotted as shown in Figure C.2. From transfer curves, the carrier density of holes in the unipolar p-type device was calculated.

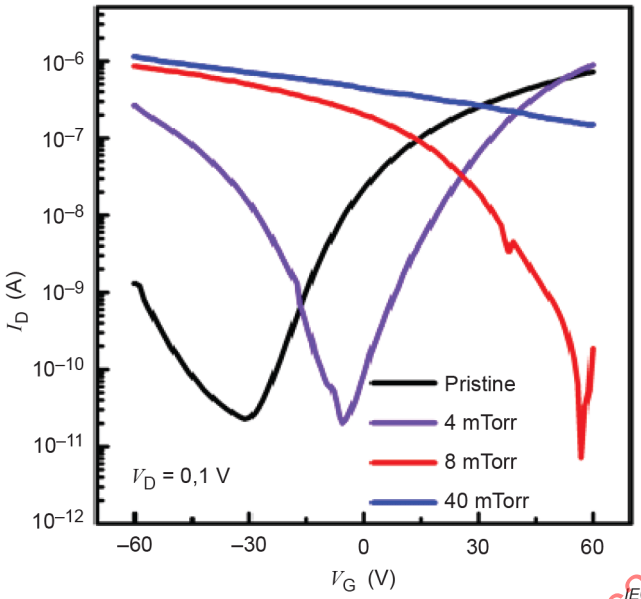


NOTE The transfer curve is obtained at the middle two electrodes of the four-probe device, with a channel length and width of 1,4 µm and 1,8 µm, respectively. The flake thickness is confirmed to be 11 nm. The dashed line shown in the upper figure indicates the line scanned for atomic force microscopy (AFM) in the lower figure.

SOURCE: Reproduced from D. Qu et al. (2017) [7], with the permission of Wiley-VCH.

Figure C.1 – Optical microscopic image of $MoTe_2$ FET and the thickness of 2D $MoTe_2$ measured by AFM

Transfer characteristics of the FET devices annealed in a rapid thermal annealing (RTA) chamber at different vacuum levels are shown in Figure C.2. Multilayer $MoTe_2$ prepared using the mechanical exfoliation method was placed on a highly doped p-Si substrate capped with a 285 nm thermally oxidized SiO_2 layer. A 5 nm/50 nm thick Cr/Au layer was then deposited onto the $MoTe_2$ flake to form the source and drain contacts using an electron beam evaporator.



SOURCE: Reproduced from D. Qu et al. (2017) [7], with the permission of Wiley-VCH.

Figure C.2 – Voltage shift observed from transfer curves measured by using 2D $MoTe_2$ FET

C.2 Test report

From Figure C.2, the carrier density of holes in the unipolar p-type device was calculated as $n_{2D} = C_g \Delta V / e$. The maximum hole carrier density reached 5 × 10^{12} cm^{-2}. [7]